1900

10.4.1.1. External Link Entry Format

Bit	*Function*	*Description*
17–0	BURST ADDR 0	Burst Address 0.
21–18	BURST LEN 0	Burst Length 0.
41–22	BURST ADDR 1	Burst Address 1.
45–42	BURST LEN 1	Burst Length 1.
65–46	BURST ADDR 2	Burst Address 2.
69–66	BURST LEN 2	Burst Length 2.
70	INT/EXT	Internal/External
71	PAR	Parity Bit. Set so that there is odd parity across bits 71:0 of the entry data.

FIG. 19

2000

10.4.1.2. Internal Link Entry Format

Bit	*Function*	*Description*
20–0	BURST ADDR 1	Burst Address 1.
25–21	BURST LEN 1	Burst Length 1.
46–26	BURST ADDR 2	Burst Address 2.
51–47	BURST LEN 2	Burst Length 2.
62–52	INT RECIPE INDEX	Internal Recipe Index.
67–63	INT RECIPE LEN	Internal Recipe Length.
69–68	—	Reserved.
70	INT/EXT	Internal/External
71	PAR	Parity Bit. Set so that there is odd parity across bits 71:0 of the entry data.

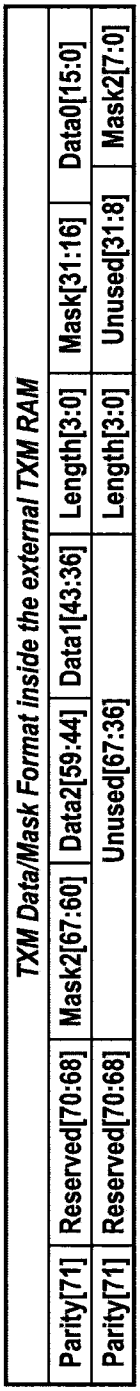
FIG. 20

2100

10.4.1.4. Data Entry Format

Bit	*Function*	*Description*
31–0	DATA 0	Data Segment 0.
35–32	DATA LEN	Data Length.
67–36	DATA 1	Data Segment 1.
70–68	—	Reserved.
71	PAR	Parity Bit. Set so that there is odd parity across bits 71:0 of the entry data.

FIG. 21A



TXM Data/Mask Format inside the external TXM RAM							
Parity[71]	Reserved[70:68]	Mask2[67:60]	Data2[59:44]	Data1[43:36]	Length[3:0]	Mask[31:16]	Data0[15:0]
Parity[71]	Reserved[70:68]	Unused[67:36]			Length[3:0]	Unused[31:8]	Mask2[7:0]

FIG. 21B

Internal Recipe RAM Data Format				
[71]	[70]	[69:36]	[35:34]	[33:0]
Parity	Command (n+1) valid	Command (n+1)	Reserved	Command(n)

FIG. 22